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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/524,408	03/13/2000	Kanad Chakraborty	YO999-598	7403

21254 7590 01/05/2005

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EXAMINER	
GARCIA OTERO, EDUARDO	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 01/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/524,408	CHAKRABORTY ET AL.	
	Examiner	Art Unit	
	Eduardo Garcia-Otero	2123	

-- The MAILING DATE of this communication appears n the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 September 2004 and 05 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3,5,6,12,13,24,26,27,33,34 and 40-55* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3,5,6,12,13,24,26,27,33,34 and 40-55* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION: Final Action

Introduction

1. Title is: METHOD AND APPARATUS FOR APPLYING FINE GRAINED TRANSFORMS DURING PLACEMENT SYNTHESIS INTERACTION
2. First named inventor is: CHAKRABORTY
3. Claims 3, 5, 6, 12, 13, 24, 26, 27, 33, 34, and 40-55 are pending.
4. US Application was filed 03/13/00, and there are no claims for earlier priority.
5. This action is in reply to Applicant's Amendment received 9/24/04, and change of address received 11/5/04.

Index of Important Prior Art

6. Shenoy refers to US Patent 6,378,114.
7. Smith refers to HDL Chip Design, by Douglas J. Smith, Dune Publications, 1996, pages 2-19.

Definitions

8. **Optimization** is defined as "[MATH] The maximizing or minimizing of a given function possibly subject to some type of constraints. [SYS ENG] 1. Broadly, the efforts and processes of making a decision, a design, or a system as perfect, effective, or functional as possible. 2. Narrowly, the specific methodology, techniques, and procedures used to decide on the one specific solution in a defined set of possible alternatives that will best satisfy a selected criterion. Also known as system optimization." by McGraw–Hill Dictionary of Scientific and Technical Terms, Fourth Edition, page 1329, 1989.
9. **Simulation** is defined as "the imitation of the operation of a real-world process or system over time. Simulation involves the generation of an artificial history of the system and the observation of that artificial history to draw inferences concerning the operating characteristics of the real system that is represented. Simulation is an indispensable problem-solving methodology for the solution of many real-world problems. Simulation is used to describe and analyze the behavior of a system, ask what-if questions about the real system, and aid in the design of real systems. Both existing and conceptual systems can be modeled with simulation." by The Handbook of Simulation, Jerry Banks, 1998, pages 3-4.

Preliminary Discussion of Specification and Drawings

10. A preliminary discussion of the specification and drawings is useful before addressing Applicant's Remarks.

11. THREE SEPARATE DOMAINS. Applicant presents an interesting broad conceptual approach to integrated circuit design, whereby the circuit design space (the universe of all possible circuit designs) is defined by three separate domains at Specification page 5 lines 3-4: "in Figure 1, the three axes represent optimizations along Boolean, electrical and physical domains". Said broad conceptual approach is very useful for broad conceptual or theoretical discussions.

12. However, Applicant's broad representation of circuit design space has limited direct application in a practical optimization environment, because the three domains interact in a complex, non-linear, and unpredictable fashion. See Shenoy Column 1. Optimizing in one domain generally degrades another domain in a non-linear and unpredictable complex fashion. For example, circuit elements (transistors) with larger areas are faster (electrical domain), but take more layout area (physical domain). Thus, Applicant's representation of the prior art's sequential optimization as traveling sequentially from point to point in directions parallel with the axes (specification page 5 and FIG 1 points A-F) is not fully accurate because the axes are interactive.

13. Note that optimization in a single domain will simultaneously affect the other domains. For example, the electrical and physical domains are directly related, as discussed in the transistor example above. The Boolean domain is slightly different because the electrical and physical domains may be changed without changing the Boolean domain. However, any change in the Boolean domain will always change both the physical and electrical domains. See Shenoy column 1.

14. Further, Specification page 9 line 17 states that "a single step may optimize the physical, Boolean and electrical dimensions, thus moving the design from point A to F' in the design space. Multiple steps are not required". This broad assertion is not supported. Consider a simple illustrative example: first the Boolean space is changed, then this change is propagated to the electrical domain (new electrical elements to implement the new Boolean logic, and new basic characteristics of the new electrical elements), and then propagated to

the physical (layout) domain, and then propagated to the electrical domain again (capacitance of connecting lines, noise from connecting lines, and related electrical characteristics that are dependent upon the layout of the electrical elements). See Shenoy column 1. This simple example illustrates the key point that changes to a single domain must be propagated sequentially to the other domains, and that the "overall design" (Shenoy column 1 line 66) is optimized, and all three domains are not optimized simultaneously.

15. COMPLEXITY OF INTEGRATED CIRUITS. Modern integrated circuits are probably the most complex creations of man. They contain millions of individual electrical elements, tightly packed into three dimensions, with electric charges generating electric fields, and with moving charges generating magnetic fields, with heat being generated and dissipated, with logical operations occurring, and with all of these chemical, electrical, logical, quantum semiconductor, and thermal phenomenon interacting in space and in time at frequencies of millions or billions of cycles per second. Thus, the design and optimization of integrated circuits is highly unpredictable. See the Wands 8 factor test regarding undue experimentation, particularly factor (7) "the predictability or unpredictability of the art", *In re Wands* (CA FC) 8 USPQ2d 1400, 1404 (9/30/1998).
16. ITERATIVE OPTIMIZATION. Smith discloses the state of the art. Specifically, note the hierarchical and iterative nature of integrated circuit design and optimization at Figure 1.3 page 7 and Figure 1.14 page 19. Further, note the various behavioral levels of abstraction displayed at Figure 1.5: System, Algorithm, RTL (Register Transfer Level), Logic, and Gate.

Applicant's Remarks

17. OPTIMIZATION. Remarks page 8. Applicant asserts "It is determined whether the considered netlist modification and the considered cell placement improve the design space. If so, then the netlist modification and cell placement are implemented; but if not, a different netlist modification and cell placement are considered". Emphasis in original.
18. This appears to be disclosed by Shenoy at column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32

"after cell separation is performed, the netlist is tweaked to optimize the design". See Shenoy FIG 1.

19. Note that the McGraw-Hill Dictionary definition for "optimization" is "[MATH] The maximizing or minimizing of a given function possibly subject to some type of constraints. [SYS ENG] 1. Broadly, the efforts and processes of making a decision, a design, or a system as perfect, effective, or functional as possible. 2. Narrowly, the specific methodology, techniques, and procedures used to decide on the one specific solution in a defined set of possible alternatives that will best satisfy a selected criterion. Also known as system optimization."
20. MULTIPLE CRITERIA. Remarks page 9. Applicant addresses the issue of multiple criteria optimization. Shenoy also discloses multiple criteria optimization for cell placement and netlist.

35 USC § 112-Second Paragraph-indefinite claims

21. The following is a quotation of the second paragraph of 35 U.S.C. 112: The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
22. Claims 3, 6, 12, 41 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
23. In claim 3, the term "the netlist modification is divided into a set of steps, each step addressing a specific aspect of the design space" is not clear. Please define "set of steps" and "aspect of the design space".
24. In claim 6, the term "logical data" is not clear. Possibly this term is related to the Boolean dimension of FIG 1.
25. In claim 12, the terms "predetermined stages" and "implement" are not clear. Please clarify either what these stages are, or else how to determine them. Please define "implement".
26. In claim 41, the term "considering a cell placement comprises considering a plurality of placement techniques" is not clear. Please define this "plurality of placement techniques", and explain how a plurality of placement techniques can be considered simultaneously.

35 USC § 102(e): filed before 11/29/00 and not vol. pub. under 35 USD 122(b)

27. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action: A person shall be entitled to a patent unless – (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

28. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

29. Claims 3, 5, 6, 12, 13, 24, 26, 27, 33, 34, and 40-55 are rejected under 35 U.S.C. 102(e) as anticipated by Shenoy US Patent 6,378,114.

30. Claim 40 is rejected under 35 U.S.C. 102(e) as anticipated by Shenoy US Patent 6,378,114.

31. Claim 40 is an independent "method" claim with 4 limitations, labeled by the Applicant as (a) through (d).

32. "**(a) considering a possible netlist modification for the design space**" is disclosed by Shenoy at column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design", and FIG 1.

33. "**(b) considering a cell placement for the modified netlist**" is disclosed by Shenoy at column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design", and FIG 1.

34. "**(c) determining whether the considered netlist modification and the considered cell placement improve the design space**" is disclosed by Shenoy at column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column

3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design", and FIG 1.

35. "**(d) if the considered netlist modification and the considered cell placement improve the design space, implementing the considered netlist modification and the considered cell placement, but if the considered netlist modification and the considered cell placement to do not improve the design space, returning to (a)**" is disclosed by Shenoy at column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design", and FIG 1.
36. Note that the McGraw-Hill Dictionary definition for "optimization" is "[MATH] The maximizing or minimizing of a given function possibly subject to some type of constraints. [SYS ENG] 1. Broadly, the efforts and processes of making a decision, a design, or a system as perfect, effective, or functional as possible. 2. Narrowly, the specific methodology, techniques, and procedures used to decide on the one specific solution in a defined set of possible alternatives that will best satisfy a selected criterion. Also known as system optimization."
37. Claims 3, 5, 6, 12, 13, and 41-45 depend from independent claim 40.
38. In claim 3, **"the netlist modification is divided into a set of steps, each step addressing a specific aspect of the design space"** is disclosed by Shenoy at column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design", and FIG 1.
39. In claim 5, **"the modification optimizes the combination of the physical, Boolean and electrical domains"** is disclosed by Shenoy at column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design", and FIG 1.

40. In claim 6, **"the modification affects multiple objectives and constraints which involve physical placement, electrical properties, and logical data"** is
41. In claim 12, **"at predetermined stages of the method, selectively determining whether to intercept the method and implement the most recently considered netlist modification and cell placement"** is disclosed by Shenoy at column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design", and FIG 1.
42. In claim 13, **"examining a plurality of domains to find an improved design, said examining comprising evaluating the effects of the considered netlist modification and cell placement on design targets"** is disclosed by Shenoy at column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design", and FIG 1.
43. Note that the McGraw-Hill Dictionary definition for "optimization" is "[MATH] The maximizing or minimizing of a given function possibly subject to some type of constraints. [SYS ENG] 1. Broadly, the efforts and processes of making a decision, a design, or a system as perfect, effective, or functional as possible. 2. Narrowly, the specific methodology, techniques, and procedures used to decide on the one specific solution in a defined set of possible alternatives that will best satisfy a selected criterion. Also known as system optimization."
44. In claim 41, **"wherein considering a cell placement comprises considering a plurality of placement techniques"** is disclosed by Shenoy at column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design", and FIG 1.
45. In claim 42, "the design space is divided into bins, and (a) through (c) are performed on a bin" is disclosed by Shenoy at abstract "plurality of partitions".

46. In claim 43, **"determining whether further improvement of the design space should be sought; and if so, returning to (a)"** is disclosed by Shenoy at column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design", and FIG 1.
47. Note that the McGraw-Hill Dictionary definition for "optimization" is "[MATH] The maximizing or minimizing of a given function possibly subject to some type of constraints. [SYS ENG] 1. Broadly, the efforts and processes of making a decision, a design, or a system as perfect, effective, or functional as possible. 2. Narrowly, the specific methodology, techniques, and procedures used to decide on the one specific solution in a defined set of possible alternatives that will best satisfy a selected criterion. Also known as system optimization."
48. In claim 44, **"making an initial layout for the design space"** is disclosed by Shenoy at column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design", and FIG 1.
49. In claim 45, **"storing information to update data about the implemented netlist and cell placement"** is disclosed by Shenoy at Abstract "computer controlled" and column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design", and FIG 1.
50. Claims 24, 26, 27, 33, 34, and 46-49 are "system" (machine) type claims with the same limitations as "method" claims 3, 5, 6, 12, 13, and 41-45, and thus are rejected for the same reasons.
51. Claims 50-55 are "programmable storage medium" type claims with the same limitations as "method" claims 3, 5, 6, 12, 13, and 41-45, and thus are rejected for the same reasons.

Response to Amendments or new IDS-FINAL OFFICE ACTION

52. Applicant's amendments or new IDS necessitated the new ground(s) of rejection presented in this Office action. Accordingly, THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Additional Cited Prior Art

53. The following US patents or publications are hereby cited as prior art, but have not been used for rejection. Applicant should review these carefully before responding to this office action.

54. HDL Chip Design, by Douglas J. Smith, Dune Publications, 1996, pages 2-19 disclose the state of the art. Specifically, note the hierarchical and iterative nature of integrated circuit design and optimization at Figure 1.3 page 7 and Figure 1.14 page 19. Further, note the various behavioral levels of abstraction displayed at Figure 1.5: System, Algorithm, RTL (Register Transfer Level), Logic, and Gate.

Conclusions

55. All pending claims stand rejected.

Communication

56. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eduardo Garcia-Otero whose telephone number is 571-272-3711. The examiner can normally be reached on Monday through Thursday from 9:00 AM to 8:00 PM. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kevin Teska, can be reached at 571-272-3761. The fax phone number for this group is 703-872-9306.

* * * *

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER